A Qualitative Approach on FinFET Devices Characteristics

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Abstract—FinFET devices are comprehensively investigated owing to the projection for application in the CMOS integrated circuits fabrication. Deducing MOSFET size have great influence on electrostatic characteristic. The indiscriminate variations of the characteristics lead to a divergence effect which is imperative from the point of view of design and manufacture. In this paper different types of the possible variations of FinFET characteristics are discussed. We have considered only n-channel devices. The behavior of hole mobility in multigate devices is of course of great importance.[1-2]. We discuss simulation study on electron mobility in FinFET with electric field applied. Mobility enhancement is observed in devices with thinner silicon film, when higher field is applied, which can be attributed to "volume inversion" in FinFET.

Index-Terms—FinFET, mobility, electrical characteristics.

INTRODUCTION: The continuing scaling of CMOS (Complementary Metal-Oxide-Semiconductor) technology requires noteworthy innovations in different fields, from short channel effect restraint to carrier transport improvement [3-7]. As devices get smaller further and further, the problem with conventional MOSFETs are increasing. We are facing several problem such as \( V_T \) rolloff, drain induced barrier lowering (DIBL), increasing leakage current and so on. Solving one problem leads to another. To solved the problem several MOSFET has been introduced such as double gate, FinFET, Trigate, Foregate, All around gate and so on. We will discuss here the electrostatic characteristic of FinFET such as current – voltage curves, mobility variation with electric field on MOSFET. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the gate of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. It is very important to know the characteristics of MOSFET to work properly from this aspect we tried to discuss the qualitative feature of FinFET characteristics.

THEORY: All the MOSFET characteristics are expressed as functions of the values of the surface potential at the source and drain ends. In the threshold voltage approach separate solutions are available for different regions of MOSFET operation (Fig. 1). For FinFET

![Device structure used in this study](image)

**Linear Region.** It is the region in which \( I_{ds} \), increases linearly with \( v_{ds} \), for a given \( v_g \) (\( > v_T \)). To a first approximation, \( I_{ds} \), in the linear region is given by

\[
I_{ds} = 2 \mu C_{ox} \frac{W}{L} \left( v_g - v_T - \frac{v_{ds}}{2} \right) v_{ds}
\]

where \( \mu \) is mobility of the carriers (electrons for nMOST) in the channel (inversion) region, \( C_{ox} \) is the
gate oxide capacitance per unit area, $W/L$ is device width to length ratio and $V_t$ is threshold voltage.

**Saturation Region.** In this region $I_{ds}$ no longer increases as $V_{ds}$ increases. Once more to a first rough calculation, $I_{ds}$ in the saturation region is given by

$$I_{ds} = \mu C_{ox} \frac{W}{L} \left( \frac{V_g - V_t}{2m} \right)^2$$

Where, $m=1+\frac{3t_{ox}}{X_d}$

$X_d$ is the depletion layer thickness and $t_{ox}$ is the oxide thickness.

showing that $I_{ds}$, does not depend on $V_{ds}$ This is evident from Figure 3.4

**Cut-Off Region.** This is the region where $V_g < V_t$, so that no channel subsist between the source and the drain, consequential in $I_{ds} = 0$. In fact for $V_g < V_t$, drain current follows an exponential decompose is referred to subthreshold current. The low electron concentration results in low electric field along the channel and as a result the subthreshold current is primarily owing to diffusion of carriers. The current in subthreshold region is approximated as

$$I_{ds} = \mu \frac{W}{L} kT n_i t_{sl} e^{\frac{q(V_g - \Delta \phi)}{kT}} e^{-\frac{qV_{ds}}{kT}}$$

$\Delta \phi$ is the work function difference between the gate electrode and the almost intrinsic silicon body

The MOSFET characteristics shown in Figures 1 is often called output characteristics while those shown in Figure 2 and 3 are called transfer characteristics. The threshold Voltage, $V_t$ for FinFET is:

$$V_{th} = \phi + \frac{n kT}{q} \ln \left( \frac{2 C_{ox} kT}{q^2 n_i t_{sl}} \right) + \frac{h^2 \pi^2}{2 m_{ds} W_{si}}$$

The applied Effective electric field, $E_{eff}$ is defined as

$$E_{eff} = \frac{1}{2} \frac{q}{e} \left( \frac{N_{inv}}{2} + N_{sub} \times t_{sl} \right)$$

The mobility is resolute by numerous scattering mechanisms through which the carriers exchange momentum with the semiconductor. the scattering mechanisms are owed to the imperfections of the semiconductor crystal, namely lattice vibrations, ionized impurity atoms, and interface related imperfections, such as surface roughness and interface trapped charges. The mobility in the inversion channel has long been a subject of powerful examination [8]. In the scrupulous case of the MOSFET, three mechanisms combine to determine the overall mobility, namely

Coulomb scattering, $\mu_{col} = \mu_0 \left( 1 + \frac{E_{eff}}{e_{col}} \right)^n$phonon scattering, $\mu_{ph} = \frac{\mu_0^p}{(1 + \frac{E_{eff}}{e_{ph}})^n}$

and surface roughness scattering, $\mu_{sr} = \mu_0^s \left( \frac{E_{eff}}{e_{eff}} \right)^y$

[9], [10], [11], [12]. These three factors that contribute to the total mobility can be combined using Matthiesen’s rule [11], which states that

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{col}} + \frac{1}{\mu_{sr}}$$

In equation (A), $\mu_{eff}$ is the total mobility and the factors in the right-hand side of (A) represent the phenomena contributing to mobility. Figure 4. shows the dependence of the inversion layer mobility on the average electric field.

**RESULTS:** Most important Features of FinFET are:

1. Ultra thin Si fin for suppression of short channel effects. (2) Raised source/drain to reduce parasitic resistance and improve current drive. (4) Symmetric gates yield great performance, but can built asymmetric gates that target $V_T$. (5) FinFETs are designed to use multiple fins to achieve larger channel widths.Source/Drain pads connect the fins in parallel. As the number of fins is increased ,the current through the device increases. For eg: A 5 fin device 5 times more current than single fin device. (6) The main advantage of the FinFET is the ability to drastically reduce the short channel effect. In spite of his double-gate structure, the FinFET is closed to its root, the conventional MOSFET in layout and fabrication.
Fig. 1. show the output characteristics of FinFET of Lch=10µm, Wfin=150nm, tsi=30nm for various gate voltage.

Fig.1. Indicate increasing drain current with increasing drain voltage this condition is true upto pinch off voltage then there is no effect of drain voltage over drain current.

Fig.2. Transfer characteristics of FinFET of
(a) Lch=10µm, Wfin=150nm, tsi=30nm
(b) Lch=100.2nm, Wfin=60nm, tsi=20nm

Fig.2 Tell us there is no current flowing upto threshold voltage but after this voltage current start increasing. This is ideal condition. In practical situation current flow before threshold voltage reaching.

Fig.3. Subthreshold current of n-Channel FinFET of Lch=10µm Wfin=150nm, tsi=30nm.

This figure indicate the Subthreshold current of n-Channel FinFET where current flowing though threshold voltage did not cross.
Coulomb scattering from ionized impurities as well as charged defects near and at the interface. Coulomb scattering is more important for low electric fields, becoming less effective for higher fields due to carrier screening.

Phonon scattering is caused by the interaction of carriers with lattice vibrations. Increasing temperatures make the carrier-phonon interaction more intense, thus decreasing the mobility component due to phonon scattering.

Surface roughness scattering from deviations of the Si-SiO₂ interface from an ideal flat plane which displays a strong dependence on the effective field. Strong fields pull carriers toward the surface, making surface roughness the dominant scattering contributing to mobility degradation with strong fields.

At room temperature (300 K): For light inversion, Coulomb and phonon scattering dominate. For heavy inversion, surface roughness and phonon scattering dominate.

Big compensation of FinFET.

1. Having excellent control of short channel effects in submicron regime and making transistors still scalable. Due to this reason, the small- length transistor can have a larger intrinsic gain compared to the bulk counterpart.

2. Much Lower off-state current compared to bulk counterpart.

Promising matching behavior

CONCLUSION: Trigate FinFET has been projected as a gifted alternative for bulk CMOS technology to continue the technology scaling. This paper studies the characteristics of trigate FinFET from various aspect. FinFET circuits can achieve lower functional voltage supply and lower optimal energy consumption compared to CMOS circuits. In addition, FinFET has better immunity to soft error in sub-threshold region. Actually FinFET is more suitable and reliable for circuit design.

REFERENCES:


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